CLAIMS

What is claimed is:

1. An integrated device with a corrosion-resistant capped bond pad, comprising:

at least one aluminum bond pad on a semiconductor substrate;

a layer of electroless nickel disposed on the aluminum bond pad;

a layer of electroless palladium disposed on the electroless nickel; and

a layer of immersion gold disposed on the electroless palladium.

2. The integrated device of claim 1 wherein the integrated device is selected from the group consisting of an integrated circuit, an analog circuit, a digital circuit, a radio-frequency device, a semiconductor sensor, an integrated sensor, a pressure sensor, a microelectromechanical device, a microoptoelectromechanical device, a sensor assembly, an integrated circuit assembly, a wire-bonded assembly, and a combination thereof.

3. The integrated device of claim 1 wherein the semiconductor substrate comprises one of a silicon wafer or a silicon die.

4. The integrated device of claim 1 wherein the layer of electroless nickel is formed on the aluminum bond pad by a zinc displacement plating process.

5. The integrated device of claim 1 wherein the layer of electroless nickel has a thickness between 0.5 microns and 7.5 microns.

6. The integrated device of claim 1 wherein the layer of electroless palladium has a thickness between 0.2 microns and 1.0 micron.

7. The integrated device of claim 1 wherein the layer of immersion gold has a thickness between 0.05 microns and 0.25 microns.

8. The integrated device of claim 1 further comprising:

a layer of electroless gold disposed on the immersion gold.

9. The integrated device of claim 8 wherein the layer of electroless gold has a thickness between 0.1 microns and 1.5 microns.

10. A method of forming a capped bond pad, comprising:

providing a plurality of aluminum bond pads on a semiconductor substrate;

zincating a surface of the aluminum bond pads;

plating a layer of electroless nickel on the zincated surface of the aluminum bond pads, wherein the zincated surface is displaced with the layer of electroless nickel;

plating a layer of electroless palladium on the electroless nickel; and

plating a layer of immersion gold on the electroless palladium.

11. The method of claim 10 wherein the provided semiconductor substrate comprises one of a silicon wafer or a silicon die.

12. The method of claim 10 wherein the layer of electroless nickel is plated to a thickness between 0.5 microns and 7.5 microns.

13. The method claim 10 wherein the layer of electroless palladium is plated to a thickness between 0.2 microns and 1.0 micron.

14. The method of claim 10 wherein the layer of immersion gold is plated to a thickness between 0.05 microns and 0.25 microns.

15. The method of claim 10 further comprising:

plating a layer of electroless gold on the immersion gold.

16. The method of claim 15 wherein the layer of electroless gold is plated to a thickness between 0.1 microns and 1.5 microns.

17. A semiconductor wafer with a plurality of capped bond pads, comprising:

a plurality of aluminum bond pads on a surface of the semiconductor wafer;

a layer of electroless nickel disposed on the aluminum bond pads;

a layer of electroless palladium disposed on the electroless nickel; and

a layer of immersion gold disposed on the electroless palladium, wherein the layer of electroless nickel is formed on the aluminum bond pad by a zinc displacement plating process.

18. The semiconductor wafer of claim 17, wherein the semiconductor wafer comprises a silicon substrate.

19. The semiconductor wafer of claim 17, wherein the semiconductor wafer comprises an integrated device selected from the group consisting of an integrated circuit, an analog circuit, a digital circuit, a radio-frequency device, a semiconductor sensor, an integrated sensor, a pressure sensor, a microelectromechanical device, a microoptoelectromechanical device, a wire-bondable device, and a combination thereof.

20. The semiconductor wafer of claim 17, further comprising:

a layer of electroless gold disposed on the immersion gold.

21. A capped bond pad for a corrosion-resistant integrated device, comprising:

a layer of electroless nickel disposed on at least one aluminum bond pad;

a layer of electroless palladium disposed on the electroless nickel; and

a layer of immersion gold disposed on the electroless palladium, wherein the layer of electroless nickel is formed on the aluminum bond pad by a zinc displacement plating process.

22. The capped bond pad of claim 21 further comprising:

a layer of electroless gold disposed on the immersion gold.